RL-TR-92-149
In-House Report
September 1992

ANALOG VERY LARGE SCALE INTEGRATION (VLSI) IMPLEMENTATIONS OF ARTIFICIAL NEURAL NETWORKS

Michael L. Hinman

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REPORT DOCUMENTATION PAGE

Form Approved
OMB No. 0704-0188

1. AGENCY USE ONLY (Leave Blank)	2. REPORT DATE	3. REPORT TYPE AND DATES COVERED
	September 1992	In-House Oct 91 - Apr 92

4. TITLE AND SUBTITLE
ANALOG VERY LARGE SCALE INTEGRATION (VLSI) IMPLEMENTATIONS OF ARTIFICIAL NEURAL NETWORKS

5. FUNDING NUMBERS
PE - 62702F
PR - 4594
TA - 18
WU - N3

6. AUTHOR(S)
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7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)
Rome Laboratory (IRRP)
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Griffiss AFB NY 13441-4114

8. PERFORMING ORGANIZATION REPORT NUMBER
RL-TR-92-149

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)
Rome Laboratory (IRRP)
32 Hangar Rd
Griffiss AFB NY 13441-4114

10. SPONSORING/MONITORING AGENCY REPORT NUMBER

11. SUPPLEMENTARY NOTES
Rome Laboratory Project Engineer: Michael L. Hinman/IRRP (315) 330-3175

12a. DISTRIBUTION/AVAILABILITY STATEMENT
Approved for public release; distribution unlimited.

12b. DISTRIBUTION CODE

13. ABSTRACT (Maximum 200 words)

There has been a recent resurgence of interest in the multi-disciplinary field of artificial neural networks. Artificial neural networks, originally inspired by the computational capabilities of the human brain, refer to a variety of computing architectures that consist of massively parallel interconnections of simple processing elements. Currently, there exist two promising advanced technologies for implementing neural networks: Very Large Scale Integrated (VLSI) circuits and optical. This final technical report describes the utilization of VLSI circuits for implementing various neural networks, with an emphasis on analog VLSI. A comparison of the different implementation techniques is provided, as is the type of paradigm implemented (e.g., backpropagation, hopfield, bidirectional associative memories, etc.).

14. SUBJECT TERMS	15. NUMBER OF PAGES
Artificial Neural Networks, Analog VLSI	44
	16. PRICE CODE

17. SECURITY CLASSIFICATION OF REPORT	18. SECURITY CLASSIFICATION OF THIS PAGE	19. SECURITY CLASSIFICATION OF ABSTRACT	20. LIMITATION OF ABSTRACT
UNCLASSIFIED	UNCLASSIFIED	UNCLASSIFIED	U/L

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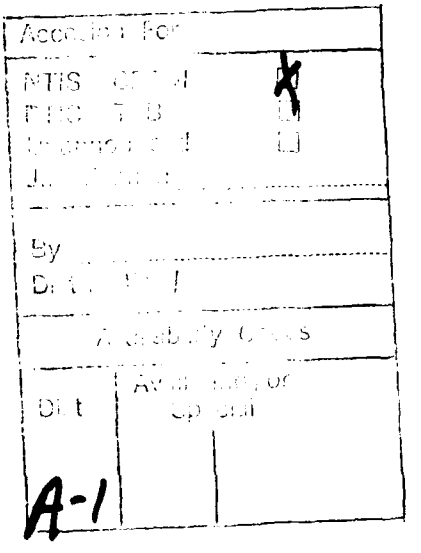

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INTRODUCTION

There has been a recent resurgence of interest in the multi-disciplinary field of artificial neural networks. Artificial neural networks, originally inspired by the computational capabilities of the human brain, refer to a variety of computing architectures that consist of massively parallel interconnections of simple processing elements.

Artificial neural networks (a.k.a. Neural Networks) are implemented utilizing a variety of technologies, as shown in Fig 1. The most used implementation technique is via computer simulations, which provide a very flexible framework from which to evaluate a particular paradigm, and for comparing with more conventional processing algorithms.

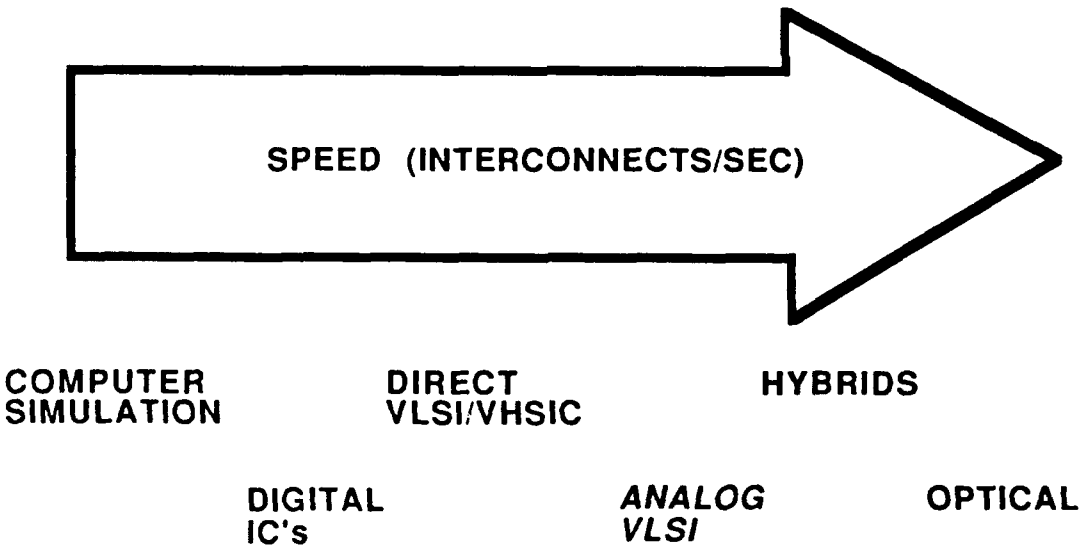

FIG 1: IMPLEMENTATIONS

However, computer simulations of neural networks, especially during training, can be exceptionally slow, even with the use of commercially available neural network accelerator boards. Also, once a hardware implementation of the neural network has been established, the comparison between it and the conventional simulation of the neural network becomes irrelevant.

Digital integrated circuit (IC) implementations offer an improvement in the processing speed of neural networks, measured in interconnections per second, but they are generally static architectures encompassing larger packaging requirements than are useful in realistic applications. Therefore, the artificial neural networks that have been implemented using digital ICs are usually limited in the number of neurons and interconnections which can be constructed primarily due to size constraints. Currently, there exist two promising advanced technologies for implementing neural networks: Very Large Scale Integration (VLSI) circuits, and optical.

This final technical report describes the utilization of VLSI circuits for implementing various neural networks, with an emphasis on *analog VLSI*, as opposed to digital VLSI, implementations. The recent literature on analog VLSI implementations of neural networks is scattered throughout a number of conference proceedings and journals, making it difficult to gain an overview of the different analog VLSI techniques utilized. This report is aimed at providing such an overview.

Several of the papers referenced have working versions of analog VLSI implementations, while others have theorized the methodology required for analog VLSI implementations. Some of the research presented incorporates a hybrid of analog and digital VLSI techniques for implementation, utilizing the advantages of each technology. A comparison of the different implementation techniques (e.g., CMOS, MOSFET, MNOS, etc.) is provided, as is the type of paradigm implemented (e.g., backpropagation, Hopfield, bidirectional associative memories, etc.).

BACKGROUND

Computation within the human brain is currently believed to be an electrochemical process which takes place in an analog fashion . The inputs to the brain are received

as a continuous (ie, analog) stream of data, such as received by the auditory and visual systems. This data is then processed by a multitude of massively interconnected biological neurons. The human cerebral cortex is believed to contain approximately 100 billion neurons, which are connected by approximately 100,000 billion synapses, providing some 10,000 billion interconnections per second [61]. The computational capability of the human brain does not depend on the ability of just one neuron, but the collective computation from billions of neurons. This enormous processing capability has provided the inspiration to a multitude of researchers to obtain a comparable computing capability, and several researchers are currently investigating the potential of advanced hardware implementations of artificial neural networks.

A simplified artificial neuron model is illustrated in Fig 2, which consists of a processing element (PE) whose output is a function of its input. The input to a

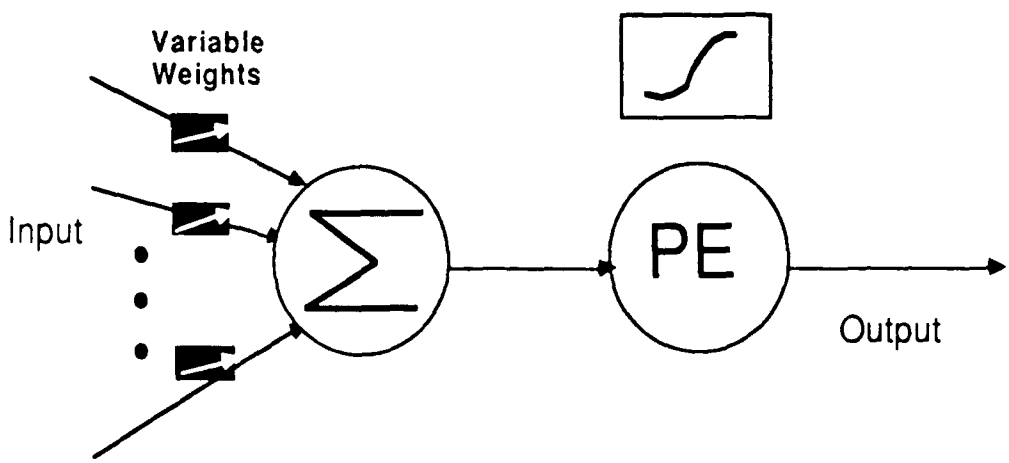

Fig 2: A Model Neuron

processing element is the weighted sum of either outputs from other PEs or the original inputs to the network. This weighted sum is then presented to the PE, which

incorporates a nonlinear transfer function (e.g., sigmoid) to determine the output, which is then presented to either other PEs or the network output. Therefore an implementation of an artificial neural network must be able to compute sums and products very efficiently.

Although artificial neural networks can be implemented using static weights, the use of variable weights, as illustrated in Fig 2, appears to be leading the charge in the research community. The hardware implementation of variable weights permits the artificial neural network to adapt or 'learn' over time. The weights are typically adapted using an equation of the form:

$$new\_weight = old\_weight + error\_correction\_term$$

Three different learning schemes, Hebbian, Least Mean Squares (LMS) or Delta Rule, and Self Organizing, all have this form [6]. As stated in [29] the most important aspect from a hardware perspective is that most learning techniques require interconnection weights that are adjustable in small steps. The ability to adjust the weights in small steps implies that high resolution is required for storing the weights. However, several researchers have shown that in the evaluation phase (feedforward, no training) most networks are very tolerant to low precision in the weights [29]. The different learning schemes can either be accomplished off-chip or on-chip, and this decision has a large impact on the actual circuit implementation based on existing technologies.

ADVANCED IMPLEMENTATION TECHNOLOGIES

There are two advanced technologies currently being researched for implementing artificial neural networks: VLSI and Optical. As stated in [61] the "principle advantage of using optics for the implementation of neural networks is the fact that one can optically implement a three-dimensional system with relative ease". An optical implementation (e.g., holographic) offers an advantage in the interconnections of the neurons in that it can be done optically, as opposed to the maze of interconnects which are required in VLSI implementations. For this reason, optics is one of the promising technologies for implementing neural networks. For more information on optical (as well as opto-electronic/hybrid) implementations, the reader is referred to the open literature.

The other promising technology for artificial neural network implementations is VLSI circuits. VSLI circuits are essentially two-dimensional (ie, planar) devices, which implies that a limited number of layers are available for the interconnection of processing elements. (It should be mentioned that, according to [24], major development in three-dimensional IC connectivity is taking place primarily in Japan.) There are two approaches to implementations based on VLSI technology, either Analog VLSI or Digital VLSI.

Digital VLSI is a mature technology from which to draw from for implementing artificial neural networks. There exists a variety of design tools (e.g., Computer Aided Design tools) which are amenable to digital VLSI circuit design, which permits circuit designers to more easily construct complex digital circuits. Also, the artificial neuron and the synapses can both easily be implemented in digital hardware, since each can be expressed by simple arithmetic operations. Another advantage of digital processing is the accuracy at which computations can be performed. The issue of accuracy also has a direct impact on the resolution of the weights, as digital implementations can have arbitrarily precise weights, which influences the training of the artificial neural network, as well as the final output. However, one of the major disadvantages of digital neural implementations is that too much silicon area is consumed [67]. Another disadvantage is that digital circuits require relatively high signal to noise ratios in order to obtain accurate results [61]. For more information on digital VLSI implementations, the reader is referred to the open literature.

Analog VLSI implementations, on the other hand, utilize much less silicon area. One of the reasons for this, is that analog computation utilizes properties of the device physics. For example, summation in an analog circuit can be accomplished by making use of the principles of Kirchoff's Current Law, which is based on the physical concept of Conversation of Charge [58]. Kirchhoff's current law states that the sum of the currents into the node is equal to the sum of the currents out of the node.Conservation of charge essentially states that electrical charge can be neither created nor destroyed; therefore a node, by itself, cannot store any charge. Summation, therefore, is obtained simply by combining the currents from other neurons onto a wire. A simplified example of an analog implementation of a model neuron [29] is shown in Fig 3, where the weighted connections from other neurons are summed along the

input wire of neuron 1. The output of neuron 1 is a voltage, which is then transmitted to other neurons through the respective connections (weights). The output voltage of

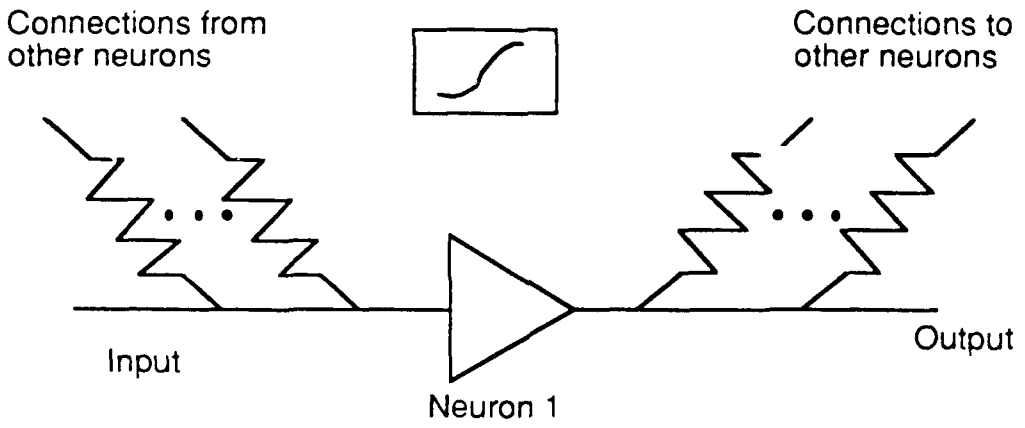

Fig 3: A Simplified Neuron Implementation

This figure extracted from Graf [29]

neuron 1 is given by the following relationship:

$$\text{Output\_Voltage} = f(\text{Input\_Current})$$

The input current to neuron 1 is equal to the sum of the currents through the connections from other neurons, where the individual currents are equal to the voltage from the respective neuron times the conductance of the connection weight. Therefore, as was previously shown, one of the basic computations to be performed by an artificial neural network is a sum of products.

For analog computation, the basic signals used are currents and voltages. As

previously described, the output of neuron 1 is a voltage. This voltage, which is supplied as the input to the connections which lead from neuron 1 to other neurons, is the same for all connections leading from neuron 1. For these reasons, analog VLSI is highly appropriate for the massively parallel implementations of artificial neural networks. Mead [58] provides an excellent description of how simple analog circuits can be implemented as building blocks to obtain results which are functionally similar to processes performed by biological systems.

Other physical properties of devices which can be useful for analog computations are natural propagation which can be used to provide time delays, and noisy devices which can be used to perform stochastic processing [61]. Another advantage of analog computation is the extremely high computational rates which can be achieved by using the physical properties of simple devices. This results in efficient utilization of silicon, thereby providing very high densities.

Some of the disadvantages of analog computation stem from the lack of sophisticated design tools such as the tools available for digital design. Another disadvantage is the accuracy of the computations, or even the accuracy at which the individual weights can be stored. The ability to retain high precision weights in an analog implementation is currently being researched, but recent results have shown that dynamic resolutions on the order of 11-12 bits are possible [19,80]. However, for the reasons listed above, there are several researchers who are utilizing a hybrid analog / digital implementation for artificial neural networks to take the advantages of each technology, while reducing the disadvantages associated with each technology. For further information on hybrid analog/digital implementations, refer to table 1 which includes references pertaining to hybrid implementations. The remainder of this report will emphasize analog VLSI implementations of artificial neural networks.

ANALOG VLSI TECHNOLOGIES/IMPLEMENTATIONS

Probably the most compelling reason to use analog VLSI for implementing artificial neural networks is that inputs obtained from the real world are analog! There currently exist a number of technologies which can be used to implement an analog (or hybrid analog / digital) VLSI based artificial neural network. Listed below are the

technologies which have appeared in the open literature:

- *Generic CMOS* (capacitors, FETs, etc.)
  (includes subthreshold MOSFET operation)
- *Floating Gate Transistors*
- *Charge-Coupled Devices (CCD)*
- *EEPROMS*
- *Metal Nitride Oxide Silicon (MNOS)*, and
- *Pulse Code Modulation* (includes Pulse Freq Modulation and Pulse Width Modulation)

Generic Complementary Metal-Oxide Semiconductor (CMOS) Technology is the principle technology used in microelectronics today. Techniques included in this category include the use of MOS capacitors for storing weights, MOSFETs (field effect transistors), and the use of subthreshold circuits as described in [58]. CMOS technology acquired its name from the concept upon which it is based. The complementary aspect is a result of the use of both p-channel and n-channel MOS transistors. P-channel MOS transistors are transistors which utilize positive charges (holes) as the charge carriers, while n-channel MOS transistors utilize negative charges (electrons) as the charge carriers. For an excellent description of CMOS VLSI technology, the reader is referred to [58]. The Generic CMOS category was the most utilized technology among the papers researched, and included the implementations for a variety of paradigms with the exception of the Kohonen net. Figs 4 & 5 illustrate the references which utilize generic CMOS technology for implementing certain paradigms / biologically inspired functions.

Fig 4 contains a wealth of information. Listed under the heading "PARADIGM" are the artificial neural network models which have been implemented by the variety of references included in this paper. Descriptions of the models are widely available in the open literature. The last two entries GENERAL and UNKNOWN however need some elaboration. The GENERAL category has been included for those hardware implementations that have either implemented more than one paradigm, or the authors have stated that they can implement a variety of different paradigms. The

PARADIGM \ TECHNOLOGY	CCD	FLOATING GATE	MNOS (EEPROM)	CMOS (MOSFET MOS CAPS)	PCM PFM PWM
ASSOCIATIVE MEMORY				[27,28,29] [30,73]	
BACKPROP	[54]	[82]		[2,3,4,25,48] [57,84]	[15,63]
BIDIRECTIONAL ASSOC MEMORY				[7,56]	
BOLTZMANN MACHINE				[3,4]	
HOPFIELD	[1,76,77]	[36]	[36,76,77]	[40,51,65] [78,86]	[43]
KOHONEN					[35]
MULTI-LAYER PERCEPTRON				[71,87]	
NEOCOGNITRON	[12]	[11]			
GENERAL	[1]	[11,36]	[36]	[19,20,21,64,79]	
UNKNOWN		[22,53]	[8,10,44,53]	[5,23,32,39,62,80]	[9,31,66,68]

Fig 4: Paradigms Implemented vs Technology

FUNCTION	VESTIBULAR-OCULAR REFLEX	NEARAL OSCILLATOR CELL	OPTICAL MOTION SENSOR
REFERENCE	[16]	[46]	[58]

FUNCTION	ELECTRONIC COCHLEA	SEEHEAR	SILICON RETINA	ADAPTIVE RETINA
REFERENCE	[47,49,58]	[58]	[58]	[59]

FUNCTION	VISUAL & MOTOR SUBSYSTEMS	ROBOTICS APPLICATIONS	CHARACTER RECOGNITION
REFERENCE	[50]	[42]	[45]

Fig 5: Biologically Inspired Applications

UNKNOWN class was added to incorporate those articles which performed a small portion of an artificial neural network (e.g., only a synapse structure was implemented, or only general theory was provided as to the methodology in which an architecture could be implemented, regardless of the paradigm).

Fig 5 provides a quick reference of those articles which have implementations which are more applications oriented (e.g., the biologically inspired work of Mead [58]).

Floating Gate Transistors (ie, analog floating gate transistors) have been implemented as adaptive nonvolatile weights. Floating gate transistors can vary charge continuously, thereby the storage cell performs in an analog fashion [26]. The dynamic range for storage devices constructed utilizing floating gate transistors is on the order of 4-6 bits. Floating gate technology has been implemented by [11,22,36,53,82] for mainly backprop and Hopfield type networks.

Charge-Coupled Devices (CCD) are structures that control the flow of charge packets [76]. Therefore CCDs can be implemented to sum charge packages, as opposed to generic CMOS processes which sum currents. Fig 6 is a schematic of the structure of a charge-coupled device.

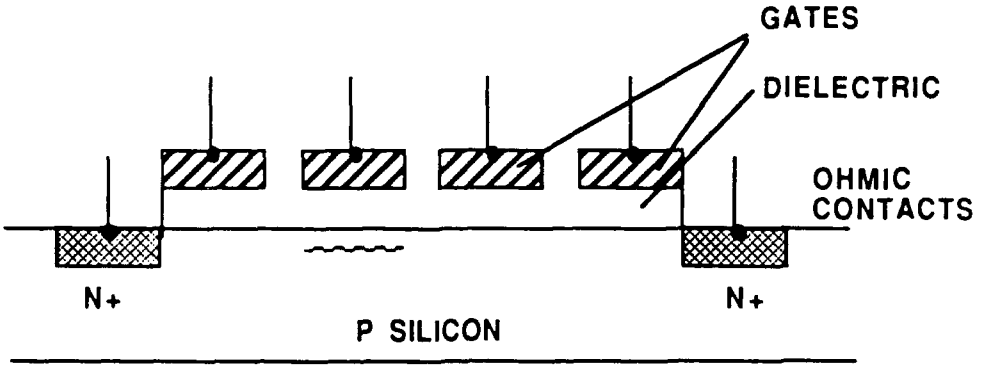

Fig 6: Schematic of the structure of a CCD

This figure extracted from Sage and Withers [76].

The operation of the CCD is described as follows: "diffusions at the beginning and end serve as sources and sinks for charge packets, whose movement through the device is controlled by voltages applied to a series of gates which are separated from the silicon by a dielectric layer" [76]. The utilization of implementations based on CCD technology have been for Backprop networks as demonstrated by Massengill and Mundie [54], Hopfield type networks as demonstrated by Sage and Withers [76], and also for different types of networks, according to Agranat [1]. A CCD architecture has also been shown to be well suited to implementing shared-weight networks (e.g., Neocognitron) by Chuang and Chiang [12].

EEPROM (Electronically Erasable Programmable Read Only Memory) technology is closely associated with floating gate transistor technology. EEPROMs offer nonvolatile storage of the synaptic weights. With EEPROMs, "the charge representing the synaptic weight is stored on the capacitance of the electronically floating gate in these devices" [10]. Some of the researchers currently investigating EEPROMs for implementing artificial neural networks includes [8,10,36,44,53,76,77]. The paradigm most often implemented is the Hopfield network, however [36] has a neural network chip currently on the market entitled ETANN (Electronically Trainable Analog Neural Network) which is capable of implementing various paradigms. For more information on ETANN, refer to the attached experimental brochure on Intel's ETANN.

Metal Nitride Oxide Silicon (MNOS) Technology was pioneered at Lincoln Laboratories. The MNOS technique permits electronic programmability, similar to EEPROM technology. MNOS devices store analog weights as charge in a nitride layer between the gate and the channel of an FET, causing a modulation of the gate voltage [67]. As described in [76] "in the conventional operation of MNOS devices using p-type silicon, the silicon surface is held either in accumulation (negative gate voltages) or in full inversion (positive gate voltages). Accumulation occurs naturally when a negative gate voltage is applied; inversion is typically allowed to occur rapidly by providing a nearby n+ diffusion as a virtually unlimited source of electrons". Examples of implementations using MNOS technology are [76,77], with the Hopfield paradigm being the model which was constructed.

Pulse Stream Arithmetic: As described in [68] , "in a pulse-stream implementation, a neuron functions as a switched oscillator. The level of accumulated neural activity

controls the oscillator's firing rate". In Murray [67,68,69], a fully analog synapse has been developed which is fully programmable, and operates on individual pulses to perform arithmetic. In Hochet, et al, [35] have implemented a Kohonen network utilizing Frequency Coded Pulse Streams. In addition, Danielli, et al, [15] and Moon, et al [63]have implemented a backpropagation network based upon Pulse Frequency/Coding Modulation.

CONCLUSION

Analog VLSI implementations of artificial neural networks is currently being investigated by a large number of researchers throughout the US, Europe, and Japan, as is evidenced by the large numbers of technical papers which have been published in a variety of conference proceedings, journals, and other technical publications.

This final technical report provides an overview of the *Analog VLSI* technologies which are currently being utilized/researched to implement artificial neural networks. Tradeoffs between analog and digital computations were presented to provide a perspective to the different approaches to computing. Shown were the relationships between the advanced analog VLSI technologies and the paradigms implemented (Fig 4), as well as the biologically inspired implementations as summarized in Fig 5. Both Figs 4 & 5 provide a concise reference to those interested in hardware implementations via analog VLSI circuits. Table 1 has been included to provide a very brief description of the references cited in this report. Table 2 has been included to provide a reference (which is by no means exhaustive) of different companies which are involved in the design of artificial neural network chips.

Ref No	Description	Learning Off-/On-Chip	Paradigms Implemented	Availability Yes/No/Exp
1	CCD technology, Fully connected neurons w/ Programmable Synapses	Off chip, 0.5ms to load weights	Hopfield	No
2	Hybrid A/D, PMOS weights, 512 neurons, limited interconnects	Off chip, 10us to load weights	Backprop	No
3	Hybrid A/D, 6 Analog neurons, 15 digital synapses (4 bits + sign)	On chip	Boltzmann & Backprop	Exp 2 micron CMOS
4	same as [3]			
5	Electronic Cascadable Learning Neural Network Chip, 32 neurons, 496 synap.	On chip		Exp
6	MOS technology	On chip (Hebbian)		No
7	Subthreshold MOSFET, with digital storage, 46 neurons, 3 layers	Off chip	BAM	Exp 3 um CMOS
8	MNOS EEPROMS, 4 neurons suitable for CMOS	Off chip	None	No
9	Hybrid A/D, Pulse Firing only 4 MOSFETs per synapse	Off chip	None	Exp
10	EEPROM weights, MOSFET channels	On chip (Hebbian)	None	No

Table 1: Brief Review of References

Ref No	Description	Learning Off-/On-Chip	Paradigms Implemented	Availability Yes/No/Exp
11	Floating Gate Matrix-vector Multipliers	On chip (Hebbian)	Multi-layer Delta Rule	Exp 2 um CMOS
12	CCD technology for shared-weight networks, digital weights, analog node values	Off chip	Neocognitron	Exp
13	4-Quadrant analog Multipliers, 10 synapse neurons, Fully Adj weights on capacitors	On chip (Hebbian)	None	Exp 2 um CMOS
14	Ferroelectric Thin Film technology	Off chip	None	No
15	Pulse Frequency Modulation, Pulse Width Modulation, Analog I/O, Asychronous	Off chip	Backprop	Exp 2 um CMOS
16	Subthreshold VLSI	On chip (unsupervised)	VOR	?
17	Hybrid Analog/Digital neural processing element, analog PSPs, digital APs		Winner-take-all	Exp 2 um n-well CMOS
18	Floating Gate MOSFETs for analog memory		None	Exp 2 um p-well CMOS
19	Analog CMOS, 3 chips: 32x32 synapse, 32 variable gain neuron, 64 input neuron	Off chip	General	Exp
20	same as [19]			
21	same as [19]			

Table 1: Brief Review of References (Cont.)

Ref No	Description	Learning Off-/On-Chip	Paradigms Implemented	Availability Yes/No/Exp
22	Floating gate MOS transistors	On chip	None	No
23	Hybrid Analog/Digital adaptive NN processor for image compression, 25x64 synapses	On chip (unsupervised)	Vector Quant, Winner-Take-All	Exp 2 um CMOS
24	Implications to Microelectronics	N/A	N/A	N/A
25	Asychronous, cascadable CMOS (10 neurons per layer, 1 layer)	Off chip	Backprop	No
26	VLSI technologies for neural networks	N/A	N/A	N/A
27	Hybrid A/D, 54 neurons-amplifiers, programmable weights, FETs	Off chip	Associative Memory	Exp 2.5 um CMOS
28	same as [27]			
29	same as [27]			
30	NET32K Chip, 256 neurons, 32K connections Analog computation, digital weights/states	Off chip	General	Exp 0.9 um CMOS
31	Hybrid A/D, Pulse Stream Synapses, 30 neurons, 120x30 synapses	Off chip		Exp 1.5 um CMOS
32	Analog CMOS implementation of discrete-time cellular neural networks	Off chip		Exp 1.5 um CMOS
33	Good review of performance measures	N/A	N/A	N/A

Table 1: Brief Review of References (Cont.)

Ref No	Description	Learning Off-/On-Chip	Paradigms Implemented	Availability Yes/No/Exp
34	Good review of performance limits	N/A	N/A	N/A
35	Frequency Coded Pulse Streams	On chip	Kohonen	Exp 2 um CMOS
36	Floating Gate nonvolatile memory (10240), EEPROM, NMOS	Off chip	Hopfield, others	Yes Intel ETANN
37	Review of VLSI implementations	N/A	N/A	N/A
38	Discrete analog implementation of multilayer perceptron (MLP) using gradient descent	On chip	MLP w/ gradient descent	No
39	MOSFETs, Binary weights	Off chip	None	Exp 3 um CMOS
40	256 neurons (op amps), programmable 2048 5 bit resistors		Hopfield-like	Exp
41	Expectation of VLSI implementations	N/A	N/A	N/A
42	Uses Silicon Retina [58] & DeWeerth Center-of-Intensity Chip for Robotics	N/A	N/A	Exp
43	Stochastic logic network (pulse-coding family) implementation of a probabilistic Hopfield		Hopfield	No
44	EEPROMs for analog weight storage	Off chip	?	Exp

Table 1: Brief Review of References (Cont.)

Ref No	Description	Learning Off-/On-Chip	Paradigms Implemented	Availability Yes/No/Exp
45	Handwritten digit recognition application	N/A	N/A	Exp
46	Uses Koch's [42] chips for Character Recognition	Off chip	Neural Oscillator Cell	Exp 3 um CMOS
47	Transconductance Amplifiers, subthreshold MOS implementation of Auditory Periphery		Auditory periphery	Exp 2 um CMOS
48	Analog implementation of MLP, MOSFET 18 neurons, 161 synapses	Off chip	MLP w/ backprop	Exp 3 um SACMOS
49	Ordinary double-metal 3 micron CMOS	N/A	Electronic Cochlea	Exp 3 um CMOS
50	Subthreshold MOS	Off chip	Visual & Motor Subsystems	Exp 2 um CMOS
51	8x8 Neural Net Controller	N/A	Hopfield	No 2 um CMOS
52	Charge Injection Multiplier Circuits, double polysilicon CMOS	N/A	Multiplier circuits	Exp 2 um CMOS
53	Multiplier Circuit, MNOS or EEPROM	N/A	Multiplier circuits	No 2 um CMOS
54	Good review of physical limitations of analog H/W; charge injection multipliers w/ EPDM	Off chip	Backprop	Exp 2 micron

Table 1: Brief Review of References (Cont.)

Ref No	Description	Learning Off-/On-Chip	Paradigms Implemented	Availability Yes/No/Exp
55	Digital Architecture, Uses INMOS Transputers	N/A	Kohonen	N/A
56	VLSI Implementation being investigated		Switched Cap. BAM (SCBAM)	No
57	Adaptive Solutions Neurocomputer Chip, digital I/O and weights	Off chip	Backprop, General	Exp
58	CMOS Building Blocks, biologically inspired		SeeHear, Silicon Retina, others	Exp
59	CMOS Building Blocks, biologically inspired	N/A	Adaptive Retina	Exp
60	Silicon gate CMOS	On chip	Adaptive Retina	Exp 2 um CMOS
61	DARPA survey on neural networks	N/A	N/A	N/A
62	PMOS Gilbert Multiplier, 2 micron p-well CMOS	N/A	Multiplier circuit	Exp 2 um CMOS
63	Pulse coding for synaptic signal weighting and summing	Off chip	Gradient descent	Exp 2 um p-well CMOS
64	same as [19]			
65	same as [19]			
66	Pulse Streams for neuron states, analog weights on capacitors	Off chip	Hopfield	Exp

Table 1: Brief Review of References (Cont.)

Ref No	Description	Learning Off-/On-Chip	Paradigms Implemented	Availability Yes/No/Exp
67	Overview of analog implementations	N/A	N/A	N/A
68	same as [66]			
69	Not VLSI oriented			
70	Differential Multiplier Method			
71	N-well CMOS, Binary weights	Off chip	Multilayer perceptron	Simulated w/ 4 um CMOS
72	Hybrid A/D network, 8x8 Hamming network, analog summation, 8 input WTA circuit		Hamming	Exp 2 um p-well CMOS
73	N-well CMOS transistors	Off chip	Associative Memory	Exp 2 um CMOS
74	Applications oriented	N/A	N/A	N/A
75	ANNA chip for character recognition, 4096 synapses, Dig I/O, Analog weights/summation	Off chip	General	0.9 um CMOS
76	MNOS analog nonvolatile weights-EEPROM, CCD for computation and control	On chip	Hopfield	Exp
77	same as [76]			
78	MOS VLSI, 4-Quadrant Multiplier, Adj Weights	On chip	Hopfield	Exp

Table 1: Brief Review of References (Cont.)

Ref No	Description	Learning Off-/On-Chip	Paradigms Implemented	Availability Yes/No/Exp
79	1024 cascadable neurons, analog weights on MOS capacitors, n-well CMOS	Off chip	Gemeral	Exp 0.9 um CMOS
80	MOS capacitors for weights (>10 bits resolution)	Off chip		Exp 1.25 um CMOS
81	Analog VLSI Splining circuit, 40 weights, analog I/O	Off chip		Exp
82	Floating gate (analog weights), CMOS process on thin film SOS	Off chip	Backprop	Exp
83	Good overview of paradigms	N/A	N/A	N/A
84	Intel's ETANN with chip-in-the-loop training	Off chip	Backprop	Yes (ETANN)
85	Non VLSI approach, good implementation			
86	14 neurons, programmable weights	Off chip	Hopfield	No 2 um CMOS
87	Double-metal p-well CMOS, feedforwad	Off chip	Multilayer perceptron	Exp 3 um CMOS

Table 1: Brief Review of References (Cont.)

Company: Accotech Chip Name: AK107 Description: Intel 8051 digital microprocessor with on-chip ROM coded for NN Availability: Now	Company: HNC Chip Name: HNC-200X Description: 2.5 billion conn/sec Availability: DARPA contract
Company: Fujitsu Ltd. Chip Name: MB4442 Description: one neuron chip, 70,000 conn/s Availability: Now in Japan	Company: Intel Corp. Chip Name: N64 (ETANN?) Description: 2.5 conn per 64x64x64 with 10,000 synapses Availability: Now
Company: Hitachi Ltd. Chip Name: None yet Description: Information encoded pulse trains Availability: Experimental	Company: Micro Devices Chip Name: MD1210 Description: fuzzy logic combined with NN in fuzzy comparator chip Availability: Now
Company: HNC Chip Name: HNC-100X Description: 100 million conn/sec Availability: Army Battlefield Computer	Company: Motorola Inc. Chip Name: None yet Description: "whole brain" chip Availability: late 1990 (?)

Table 2: Neural Network Chips

The information contained in this table was originally from an article by Colin Johnson in AI's January/February 1990 issue.
Later revised by Bruce Shriver @ USL.

Company: NASA, JPL Chip Name: None yet Description: Synapse is charge on caps that are refreshed from RAM Availability: Experimental	Company: Nippon Telephone & Telegraph Chip Name: None yet Description: Massive array of 64K one-bit processors on 1K chips Availability: Experimental
Company: NEC Corp. Chip Name: UPD7281 Description: Data flow chip set on PC board Availability: Now in Japan	Company: SAIC Chip Name: None yet Description: Information encoded pulse trains Availability: DARPA contract
Company: Nestor Inc. Chip Name: NNC Description: 150 million conn/sec 150,000 connections Availability: DoD due in 1991 (?)	Company: Systonic Systems Inc. Chip Name: Dendros-1 & -2 Description: Each has 22 synapses Availability: Now

Table 2 (cont): Neural Network Chips

The information contained in this table was originally from an article by Colin Johnson in AI's January/February 1990 issue.
Later revised by Bruce Shriver @ USL.

REFERENCES

[1] Agranat, A.J., C.F. Neugebauer, R.D. Nelson, and A. Yariv, "The CCD Neural Processor: A Neural Network Integrated Circuit with 65536 Programmable Analog Synapses", in *IEEE Transactions on Circuits and Systems,* Vol 37, No 8, pp. 1073-1075, August 1990.

[2] Akers, L.A., M. Walker, R. Grondin, and D. Ferry, "A Synthetic Neural Integrated Circuit", in *Proceedings of the IEEE 1989 Custom Integrated Circuits Conference,* pp. 12.6.1-12.6.4, May 1989.

[3] Alspector, J., B. Gupta, and R.B. Allen, "Performance of a Stochastic Learning Microchip", in *Artificial Neural Networks Electronic Implementations,* Morgan, N., Ed., IEEE Computer Society Press, Los Alamitos, CA, pp. 66-78, 1990.

[4] Alspector, J., "Neural-Style Microsystems that Learn", in *IEEE Communications Magazine,* pp. 29-36, November 1989.

[5] Alspector, J., R.B. Allen, A. Jayakumar, T. Zeppenfeld,and R. Meir, "Relaxaton Networks for Large Supervised Learning Problems", in *Advances in Neural Information Processing Systems 3(NIPS 90), Touretzky, D.S., Ed., Morgan Kaufmann,* San Mateo, CA, 1991, pp. 1015-1021.

[6] Bibyk, S., and K. Adkins, "Neural Networks and Emergent Adaptive Signal Processing", in *1989 IEEE International Symposium on Circuits and Systems,* Vol 2, pp. 1203-1206, May 1989.

[7] Boahen, K.A., et al, "A Heteroassociative Memory Using Current-Mode MOS Analog VLSI Circuits", in *IEEE Transactions on Circuits and Systems,* Vol 36, No 5, pp. 747-755, May 1989.

[8] Borgstrom, T., and S. Bibyk, "A Neural Network Integrated Circuit Utilizing Programmable Threshold Voltage Devices", in *1989 IEEE International Symposium on Circuits and Systems,* Vol 2, pp. 1227-1230, May 1989.

[9] Brownlow, M., A.F. Murray, et al, "Pulse-Firing Neural Chips for Hundreds of Neurons", in *Advances in Neural Information Processing Systems 2 (NIPS 89), Touretzky, D.S., Ed., Morgan Kaufmann,* San Mateo, CA, 1990, pp. 785-792.

[10] Card, H.C., and W.R. Moore, "Implementation of Plasticity in MOS Synapses", in *First IEE International Conference on Artificial Neural Networks,* Conference Publication Number 313, pp. 33-36, October 1989.

[11] Cauwenberghs, G., C.F. Neugebauer, and A. Yariv, "Analysis and Verification of an Analog VLSI Incremental Outer-Product Learning System", in *IEEE Transactions on Neural Networks*, Vol 3, No 3, pp. 488-497, May 1992.

[12] Chuang, M.L., and A.M. Chiang, "Simulation of the Neocognitron on a CCD Parallel Processing Architecture", in *Advances in Neural Information Processing Systems 3(NIPS 90), Touretzky, D.S., Ed., Morgan Kaufmann*, San Mateo, CA, 1991, pp. 1039-1045.

[13] Clark, J.J., "An Analog CMOS Implementation of a Self Organizing Feedforward Network", in *International Joint Conference on Neural Networks,* Vol 2, pp. 118-121, January 1990.

[14] Clark, L.T., R.O. Grondin, and S.K. Dey, "Ferroelectric Connections For IC Neural Networks", in *First IEE International Conference on Artificial Neural Networks,* Conference Publication Number 313, pp. 47-51, October 1989.

[15] Daniell, P.M., W.A.J. Waller, and D.L. Bisset, "An Implementation of Fully Analogue Sum-of-Product Neural Models in VLSI", in *First IEE International Conference on Artificial Neural Networks,* Conference Publication Number 313, pp. 52-56, October 1989.

[16] DeWeerth, S.P., and C.A. Mead, "An Analog VLSI Model of Adaption in the Vestibulo-Ocular Reflex", in *Advances in Neural Information Processing Systems 2 (NIPS 89), Touretzky, D.S., Ed., Morgan Kaufmann*, San Mateo, CA, 1990, pp. 742-749.

[17] DeYoung, M.[illegible], R.L. Findley, and C. Fields, "The Design, Fabrication, and Test of a New VLSI Hybrid Analog-Digital Neural Processing Element", in *IEEE Transactions on Neural Networks,* Vol 3, No 3, pp. 363-374, May 1992.

[18] Durfee, D.A., and F.S. Shoucair, "Comparison of Floating Gate Neural Network Memory Cells in Standard VLSI CMOS Technology", in *IEEE Transactions on Neural Networks,* Vol 3, No 3, pp. 347-353, May 1992.

[19] Eberhardt, S., A. Moopenn, and A. Thakoor, "Considerations for Hardware Implementations of Neural Networks", in *Twenty-Second Asilomar Conference on Signals, Systems, and Computers,* Vol 2, pp. 649-653, 1988.

[20] Eberhardt, S., T. Duong, and A. Thakoor, "A VLSI Analog Synapse Building-Block Chip for Hardware Neural Network Implementations", in *Third Annual Parallel Processing Symposium,* , pp. 1-11, March 1989.

[21] Eberhardt, S., T. Duong, and A. Thakoor, "Design of Parallel Hardware Neural Network Systems From Custom Analog VLSI 'Building Block' Chips", in *International Joint Conference on Neural Networks (IJCNN 1989)*, Vol 2, pp. 183-190, June 1989.

[22] El-Leithy, N., M.E. Zaghloul, and R.L. Newcomb, "CMOS Circuit for MOS Transistor Threshold Adjustment: A Means for Neural Network Weight Adjustment", in *1989 IEEE International Symposium on Circuits and Systems*, Vol 2, pp. 1221-1222, May 1989.

[23] Fang, W-C, B.J. Sheu, O.T.-C. Chen, and J.O. Choi, "A VLSI Neural Processor for Image Data Compression Using Self-Organizition Networks", in *IEEE Transactions on Neural Networks*, Vol 3, No 3, pp. 506-518, May 1992.

[24] Ferry, A., and D. Komisky, "Neural Net Development: Implications to Microelectronics Fabrication Technology", in *Proceedings of the Eighth Biennial University/Government/industry Microelectronics Symposium*, Vol 27, pp. 171-173, June 1989.

[25] Furman, B., and A.A. Abidi, "An Analog CMOS Backward Error-Propagation LSI", in *Twenty-Second Asilomar Conference on Signals, Systems, and Computers*, Vol 2, pp. 645-648, 1988.

[26] Goser, K., U. Hilleringmann, U. Ruechert, and K. Schumacher, "VLSI Technologies for Artificial Neural Networks" in *IEEE Micro Magazine*, Vol 9, No 6, pp. 28-45, December 1989.

[27] Graf, H.P., W. Hubbard, L.D. Jackel, and P.G.N. DeVegvar, "A CMOS Associative Memory Chip", in *The IEEE First International Conference on Neural Networks (IJNN 1987)*, Vol 3, pp. 461-468, June 1987.

[28] Graf, H.P., L.D. Jackel, and W.E. Hubbard, "VLSI Implementation of a Neural Network Model", in *Artificial Neural Networks Electronic Implementations*, Morgan, N., Ed., IEEE Computer Society Press, Los Alamitos, CA, pp. 34-42, 1990.

[29] Graf, H.P., and L. Jackel, "Analog Electronic Neural Network Circuits", in *IEEE Circuits and Devices Magazine*, Vol 5, No 4, pp. 44-49, July 1989.

[30] Graf, H.P., R. Janow, D. Henderson, and R. Lee, "Reconfigurable Neural Net Chip with 32K Connections", in *Advances in Neural Information Processing Systems 3(NIPS 90), Touretzky, D.S., Ed., Morgan Kaufmann*, San Mateo, CA, 1991, pp. 1032-1038.

[31] Hamilton, A., A.F. Murray, D.J. Baxter, S. Churcher, H.M. Reekie, and L.

Tarassenko, "Integrated Pulse Stream Neural Networks: Results, Issues, and Pointers", in *IEEE Transactions on Neural Networks*, Vol 3, No 3, pp. 385-393, May 1992.

[32] Harrer, H., J.A. Nossek, and R. Stelzl, "An Analog Implementation of Discrete-Time Cellular Neural Networks", in *IEEE Transactions on Neural Networks*, Vol 3, No 3, pp. 466-476, May 1992.

[33] Hecht-Nielsen, R., "Neurocomputer Interfaces and Performance Measures", in *1989 IEEE International Symposium on Circuits and Systems*, Vol 1, pp. 74-77, May 1989.

[34] Hecht-Nielsen, R., "Performance Limits of Optical, Electro-Optical, and Electronic Neurocomputers", in *SPIE Optical and Hybrid Computing*, Vol 634, pp. 277-306, March 1986.

[35] Hochet, B., V. Peiris, G. Corbaz, and M. Declercq, "Implementation of a Neuron Dedicated to Kohonen Maps with Learning Capabilities", in *Proceedings of the IEEE 1990 Custom Integrated Circuits Conference*, pp. 26.1.1-26.1.4, May 1990.

[36] Holler, M., S. Tam, H. Castro, and R. Benson, "An Electrically Trainable Artificial Neural Network (ETANN) with 10240 Floating Gate Synapses ", in *International Joint Conference on Neural Networks (IJCNN 1989)*, Vol 2, pp. 191-196, June 1989.

[37] Holler, M.A, "VLSI Implementations of Learning and Memory Systems: A Review", in *Advances in Neural Information Processing Systems 3(NIPS 90), Touretzky, D.S., Ed., Morgan Kaufmann*, San Mateo, CA, 1991, pp. 993-1000.

[38] Jabri, M., and B.Flower, "Weight Perturbation: An Optimal Architecture and Learning Technique for Analog VLSI Feedforward and Recurrent Multilayer Networks", in *IEEE Transactions on Neural Networks*, Vol 3, No 1, pp. 154-157, Jan 1992.

[39] Jenkins, R.E., "Neurodynamic Computing", in *John Hopkins APL Technical Digest*, Vol 9, No 3, pp. 232-241, 1988.

[40] Johnson, R.C.,, "Lockheed has Neural Focus", in *Electronic Engineering Times*, p 37, November 19, 1990.

[41] Kawato, M., S. Miyake, T. Inui, "Neural Networks and Expectation of VLSI Implementation", in *1988 Symposium on VLSI Circuits*, pp. 23-26, Tokyo, 1988.

[42] Koch, C., et al, "Real-Time Computer Vision and Robotics Using Analog VLSI Circuits", in *Advances in Neural Information Processing Systems 2 (NIPS 89),*

Touretzky, D.S., Ed., Morgan Kaufmann, San Mateo, CA, 1990, pp. 750-757.

[43] Kondo, Y., and Y. Sawada, "Functional Abilities of a Stochastic Logic Neural Network", in *IEEE Transactions on Neural Networks*, Vol 3, No 3, pp. 434-443, May 1992.

[44] Kramer, A., C.K. Sin, and P.K Ko, "Compact EEPROM-based Weight Functions", in *Advances in Neural Information Processing Systems 3(NIPS 90), Touretzky, D.S., Ed., Morgan Kaufmann*, San Mateo, CA, 1991, pp. 1001-1007.

[45] Le Cun, Y., L.D. Jackel, et al., "Handwritten Digit Recognition: Applications of Neural Network Chips and Automatic Learning", in *IEEE Communications Magazine*, Vol 27, No 11, pp. 41-46, November 1989.

[46] Linares-Barranco, B., et al, "A Novel CMOS Analog Neural Oscillator Cell", in *1989 IEEE International Symposium on Circuits and Systems*, Vol 2, pp. 794-797, May 1989.

[47] Liu, W., A.G. Andreou, and M.H. Goldstein, Jr., "Voiced-Speech Representation by an Analog Silicon Model of the Auditory Periphery", in *IEEE Transactions on Neural Networks*, Vol 3, No 3, pp. 477-487, May 1992.

[48] Lont, J.B., and W. Guggenbuhl, "Analog CMOS Implementation of a Multilayer Perceptron with Nonlinear Synapses", in *IEEE Transactions on Neural Networks*, Vol 3, No 3, pp. 457-465, May 1992.

[49] Lyon, R.F., and C. Mead, "An Analog Electronic Cochlea", in *Artificial Neural Networks Electronic Implementations*, Morgan, N., Ed., IEEE Computer Society Press, Los Alamitos, CA, pp. 79-94, 1990.

[50] Maher, M.C., S.P. Deweerth, M.A. Mahowald, and C.A. Mead, "Implementing Neural Architectures Using Analog VLSI Circuits", in *IEEE Transactions on Circuits and Systems*, Vol 36, No 5, pp. 643-652, May 1989.

[51] Marrakchi, A., and T. Troudet, "A Neural Net Arbitrator for Large Crossbar Packet-Switches", in *IEEE Transactions on Circuits and Systems*, Vol 36, No 7, pp. 1039-1041, June 1989.

[52] Massengill, L.W., "Multiplexed, Charge-Based Circuits for Analog Neural Systems", in *International Joint Conference on Neural Networks*, Vol 2, pp. II-88-II-91, January 1990.

[53] Massengill, L.W., "A Dynamic CMOS Multiplier for Analog Neural Network Cells",

in *Proceedings of the IEEE 1990 Custom Integrated Circuits Conference*, pp. 26.4.1-26.4.4, May 1990.

[54] Massengill, L.W., and D.B. Mundie, "An Analog Neural Hardware Implementation Using Charge-Injection Multipliers and Neuron-Specific Gain Control", in *IEEE Transactions on Neural Networks,* Vol 3, No 3, pp. 354-362, May 1992.

[55] Mauduit, N., M. Duranton, J. Gobert, and J.A. Sirat, "The Mod 2 Neurocomputer System Design", in *IEEE Transactions on Neural Networks,* Vol 3, No 3, pp. 414-422, May 1992.

[56] Maundy, B., and E.I. El-Masry, "A Novel Switched Capacitor Bidirectional Associative Memory", in *Proceedings of the IEEE 1990 Custom Integrated Circuits Conference*, pp. 26.2.1-26.2.4, May 1990.

[57] McCartor, H., "Back Propagation Implementation on the Adaptive Solutions CNAPS Neurocomputer Chip", in *Advances in Neural Information Processing Systems 3(NIPS 90), Touretzky, D.S., Ed., Morgan Kaufmann*, San Mateo, CA, 1991, pp. 1028-1031.

[58] Mead, C., *Analog VLSI and Neural Systems*, Reading, MA, Addison-Wesley, 1989.

[59] Mead, C. and M. Ismail, Ed., *Analog VLSI Implementation of Neural Systems,* Norwell, MA, Kluwer Academic, 1989.

[60] Mead, C., "Neuromorphic Electronic Systems", in *Proceedings of the IEEE,* Vol 78, No 10, pp. 1629-1636, October 1990.

[61] MIT Lincoln Laboratory, "DARPA Neural Network Study", AFCEA Press, 1988.

[62] Moon, K.K., and F.J. Kub, "Random Address 32x32 Programmable Analog Vector-Matrix Multiplier for Artificial Neural Networks", in *Proceedings of the IEEE 1990 Custom Integrated Circuits Conference*, pp. 26.7.1-26.7.4, May 1990.

[63] Moon, G., M.E. Zaghloul, and R.W. Newcomb, "VLSI Implementation of Synaptic Weighting and Summing in Pulse Coded Neural-Type Cells", in *IEEE Transactions on Neural Networks,* Vol 3, No 3, pp. 394-403, May 1992.

[64] Moopenn, A., A.P. Thakoor, T. Duong, and S.K. Khanna, "A Neurocomputer Based on an Analog-Digital Hybrid Architecture", in *The IEEE First International Conference on Neural Networks (IJNN 1987),* Vol 3, pp. 479-486, June 1987.

[65] Moopenn, A., T. Duong, and A.P. Thakoor, "Digital-Analog Hybrid Synapse Chips for Electronic Neural Networks", in *Advances in Neural Information Processing Systems 2 (NIPS 89), Touretzky, D.S., Ed., Morgan Kaufmann*, San Mateo, CA, 1990. pp. 769-776.

[66] Murray, A.F., A. Hamiltion, H.M. Reekie, and L. Tarassenko, "Pulse-Stream Arithmetic in Programmable Neural Networks", in *1989 IEEE International Symposium on Circuits and Systems*, Vol 2, pp. 1210-1212, May 1989.

[67] Murray, A.F., "Silicon Implementations of Neural Networks", in *First IEE International Conference on Artificial Neural Networks*, Conference Publication Number 313, pp. 27-32, October 1989.

[68] Murray, A.F., "Pulse Arithmetic in VLSI Neural Networks" in *IEEE Micro Magazine*, Vol 9, No 6, pp. 64-74, December 1989.

[69] Myers, D.J., and G.E. Brebner, "The Implementation of Hardware Neural Net Systems", in *First IEE International Conference on Artificial Neural Networks*, Conference Publication Number 313, pp. 57-61, October 1989.

[70] Platt, J.C., "Analog Circuits for Constrained Optimization", in *Advances in Neural Information Processing Systems 2 (NIPS 89), Touretzky, D.S., Ed., Morgan Kaufmann*, San Mateo, CA, 1990, pp. 777-783.

[71] Redman-White, W., Y.Y.H. Lam, M.D. Bedworth, and D. Bounds, Murray, "A Limited Connectivity Switched Capacitor Analogue Neural Network Processing Circuit with Digital Storage of Non-Binary Input Weights", in *First IEE International Conference on Artificial Neural Networks*, Conference Publication Number 313, pp. 42-46, October 1989.

[72] Robinson, M.E., H. Yoneda, and E. Sanchez-Sinencio, "A Modular CMOS Design of a Hamming Network", in *IEEE Transactions on Neural Networks*, Vol 3, No 3, pp. 444-456, May 1992.

[73] Rossetto, O., C. Jutten, J. Herault, and I. Kreuzer, "Analog VLSI Synaptic Matricies as Building Blocks for Neural Networks" in *IEEE Micro Magazine*, Vol 9, No 6, pp. 56-63, December 1989.

[74] Roth, M.W., "Neural-Network Technology and its Applications", in *John Hopkins APL Technical Digest*, Vol 9, No 3, pp. 242-253, 1988.

[75] Sachinger, E., B.E. Boser, J. Bromley, Y. LeCun, and L.D. Jackel, "Application of the ANNA Neural Network Chip to High-Speed Character Recognition", in *IEEE*

Transactions on Neural Networks, Vol 3, No 3, pp. 498-505, May 1992.

[76] Sage, J.P., and R.S. Withers, "Analog Nonvolatile Memory for Neural Network Implementations", in *Artificial Neural Networks Electronic Implementations,* Morgan, N., Ed., IEEE Computer Society Press, Los Alamitos, CA, pp. 22-33, 1990.

[77] Sage, J.P., R.S. Withers, and K.E. Thompson, "MNOS/CCD Circuits for Neural Network Implementations", in *1989 IEEE International Symposium on Circuits and Systems,* Vol 2, pp. 1207-1209, May 1989.

[78] Salam, F.M., N. Jhachab, M. Ismail, and Y. Wang, "An Analog MOS Implementation of the Synaptic Weights for Feedback Neural Nets", in *1989 IEEE International Symposium on Circuits and Systems,* Vol 2, pp. 1223-1226, May 1989.

[79] Satyanarayana, S., Y. Tsividis, and H.P. Graf, "A Reconfigurable Analog VLSI Neural Network Chip", in *Advances in Neural Information Processing Systems 2 (NIPS 89), Touretzky, D.S., Ed., Morgan Kaufmann,* San Mateo, CA, 1990, pp. 758-768.

[80] Schwartz, D.B., R.E. Howard, and W.E. Hubbard, "A Programmable Analog Neural Network Chip", in *IEEE Journal of Solid-State Circuits,* Vol 24, No 2, pp. 313-319, April 1989.

[81] Schwartz, D.B., and V.K. Samalam, "An Analog VLSI Splining Network", in *Advances in Neural Information Processing Systems 3(NIPS 90), Touretzky, D.S., Ed., Morgan Kaufmann,* San Mateo, CA, 1991, pp. 1008-1014.

[82] Shimabukuro, R.L., P.A. Shoemaker, and M.E. Stewart, "Circuitry for Artificial Neural Networks with Non-volitile Analog Memories", in *1989 IEEE International Symposium on Circuits and Systems,* Vol 2, pp. 1217-1220, May 1989.

[83] Simpson, P.K., *A Review of Artificial Neural Systems II: Paradigms, Applications, and Implementations,* General Dynamics, San Diego, CA, 1988.

[84] Tam, S., B.Gupta, H.A. Castro, and M. Holler, "Analog Non-Volative VLSI Neural Network Chip and Backpropagation Training", to be published in *Advances in Neural Information Processing Systems 3(NIPS 90), Touretzky, D.S., Ed., Morgan Kaufmann,* San Mateo, CA, 1991.

[85] Tank, D.W., and J.J. Hopfield, "Simple Neural Optimization Networks: An A/D Converter, Signal Decision Circuit, and a Linear Programming Circuit", in *IEEE Transactions on Circuits and Systems,* Vol CAS-33, No 5, pp. 533-541, May 1986.

[86] Verleysen, M., and P.G.A. Jespers, "An Analog VLSI Implementation of Hopfield's Neural Network" in *IEEE Micro Magazine,* Vol 9, No 6, pp. 46-55, December 1989.

[87] Walker, M., P. Hasler, and L. Akers, "A CMOS Neural Network for Pattern Association", in *IEEE Micro* , Vol 9, No 5, pp. 68-74, October 1989.